

# USB4 2.0 ENGINEERING CHANGE NOTICE FORM

**Title: Adding Timing Requirements for CLx Exit**  
**Applied to: USB4 Specification Version 2.0**

<b>Brief description of the functional changes:</b>
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Adding timing requirements for CLx exit to make sure that there are no transitions that are not covered.
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<b>Benefits as a result of the changes:</b>
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Each Router will have the ability to accurately calculate the maximum exit time from CLx.
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<b>An assessment of the impact to the existing revision and systems that currently conform to the USB specification:</b>
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None
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<b>An analysis of the hardware implications:</b>
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None
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<b>An analysis of the software implications:</b>
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None
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<b>An analysis of the compliance testing implications:</b>
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None
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## Actual Change

### (a). Table 4-33 – Transmitter Behavior in Gen 4 Training Sub-states

#### To Text:

State	Transmitter Behavior
TS2	Transmitters shall send back-to-back Gen 4 TS2. The <i>Indication</i> field shall be 3h while any receiver is executing the TxFFE negotiation. <i>Indication</i> field shall be 4h after all enabled receivers complete TxFFE negotiation and the Port is ready for Clock Switch.

### (b). 4.2.1.3.2.2 – Gen 4 Behavior

#### To Text:

During Lane Initialization a USB4 Port shall meet the following timing requirements:

- Transition to the TS2 sub-state within  $t_{Gen4TS1}$  time after entering the TS1 sub-state
- Transition to the TS3 sub-state within  $t_{Gen4TS2}$  time after entering the TS2 sub-state.

During CLx exit flow a USB4 Port shall meet the following requirements:

- Start transmitting Gen 4 TS1 with *Indication* field set to 2h within  $t_{RxLock} + t_{TrainingTransition}$  time from receiving the first Gen 4 TS1.
- Start transmitting Gen 4 TS2 with *Indication* field set to 4h within  $t_{Gen4TS2Lock} + t_{TrainingTransition}$  time after receiving the first Gen 4 TS2.
- Start transmitting Gen 4 TS3 with *Indication* field set to 5h within  $t_{LFPStoTS3}$  time after detecting the first LFPS on the USB Type-C Port

The following formulas describes  $t_{LFPStoTS3}$  for a Router Assembly with  $N_{obr}$  On-Board Retimers.

$$t_{LFPStoTS3} = t_{WarmUpCLx} + \cancel{16xtPeriod} \cancel{32xtPeriod} + 2xtStopLFPS2 + \cancel{t_{Gen4TS2Lock}} + t_{RxLock} + \cancel{4xtTrainingTransition} \cancel{3xtTrainingTransition} + N_{obr} \times (\cancel{t_{SwitchNoSSC}} + t_{OBCLxForwardLFPS})$$

#### Notes:

1.  $t_{WarmUpCLx}$  represents  $t_{WarmUpCL1}$  or  $t_{WarmUpCL2}$  for CL1 or CL2 exit ~~accordingly~~ respectively
2.  $t_{OBCLxForwardLFPS}$  represents  $t_{OBCL1ForwardLFPS}$  or  $t_{OBCL2ForwardLFPS}$  for CL1 or CL2 respectively. These values stand for the LFPS forwarding by on-board retimers in a Router Assembly as described in the USB4 Re Timer specification  
 ~~$t_{CLxForwardLFPS}$  represents  $t_{CL1ForwardLFPS}$  or  $t_{CL2ForwardLFPS}$  for CL1 or CL2 exit accordingly, as described in the USB4 Retimer Specification~~
- 2-3. A USB4 Port may meet the requirements of Table 4-33 and start transmitting Gen 4 TS1 with *Indication* field set to 2h before receiving the first Gen 4 TS1.

### (c). 4.2.1.3.2.2 – Gen 4 Behavior

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## To Text:

### Equation 4-9. CL1 Exit Time

$$t_{CL1\_Exit} = t_{WarmUpCL1} + \cancel{16x t_{Period}} \cancel{- 32x t_{Period}} + 2x StopLFPS2 + \cancel{t_{Gen4TS2Lock}} + t_{RxLock} + \cancel{N_{obr} \times (t_{SwitchNoSSC} + t_{OBCL1ForwardLFPS})} + \cancel{(-N_{Re-timer} - N_{obr}) \times (t_{SwitchNoSSC} + t_{CL1ForwardLFPS})} + 4 \times t_{TrainingTransition} + t_{ActivateSSC} + t_{SSCActivated}$$

### Equation 4-10. CL2 Exit Time

$$t_{CL2\_Exit} = t_{WarmUpCL2} + \cancel{16x t_{Period}} \cancel{- 32x t_{Period}} + 2x StopLFPS2 + \cancel{t_{Gen4TS2Lock}} + t_{RxLock} + \cancel{N_{obr} \times (t_{SwitchNoSSC} + t_{OBCL2ForwardLFPS})} + \cancel{(N_{Re-timer} - N_{obr}) \times (t_{SwitchNoSSC} + t_{CL2ForwardLFPS})} + \cancel{N_{Re-timer} \times (t_{SwitchNoSSC} + t_{CL2ForwardLFPS})} + 4 \times t_{TrainingTransition} + \cancel{t} + \cancel{t_{ActivateSSC}} + t_{SSCActivated}$$

## (d) 4.2.1.6.5.1.2 Gen 4 CL0s Exit Flow

## To Text:

A USB4 Port that is in CL0s (RX) and is not initiating an entry to CL0s (TX) shall do the following when it detects LFPS on its receiver:

1. Transmit 24 CL0s\_EXIT Ordered Sets with the *CL0s Phase* field set to 00t at the beginning of an RS-FEC block. ~~The first CL0s\_EXIT Ordered Set shall be transmitted within tTrainingTransition time after detecting the LFPS.~~ The CL0s\_EXIT Ordered Sets shall be distributed among all active transmitters.
  - a. The first CL0s\_EXIT Ordered Set shall be transmitted within tTrainingTransition time after detecting the LFPS on the USB4 Port.
  - b. The first CL0s\_EXIT Ordered Set shall be transmitted within tCL0sLFPSResponse time after detecting the LFPS on the USB Type-C Port, where

$$t_{CL0sLFPSResponse} = N_{obr} \times t_{OBCL1ForwardLFPS} + t_{TrainingTransition}$$

## (e) 4.2.1.6.5.1.2 Gen 4 CL0s Exit Flow

## To Text:

Note: The USB4 Port requirements in this specification can only be verified for Router Assemblies without On-Board Re-timers, by monitoring the USB Type-C Port associated with the USB4 Port due to lack of observability. However, for Router Assemblies with On-Board Re-timers the USB4 Ports are still expected to meet the behavior and timing requirements in this specification to satisfy the CLx exit time assumptions.

The timing requirements for a Router Assembly which includes On-Board Re-timers are subject to the following assumptions:

- Each On Board Re-timer is forwarding LFPS per direction within tOBCL1ForwardLFPS as recommended in the USB4 Re-Timer Specification. Note that the actual LFPS forwarding latency cannot be qualified for On-Board Re-Timer in Router Assemblies and only taken as an assumption for end-to-end latency calculations.

## (f). Table 4-72 – Logical Layer Timing Parameters (Version 2.0 only)

## To Text:

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Parameter	Description	Min	Max	Units
<a href="#">tGen4TS2Lock</a>	<a href="#">Time to lock on Gen 4 TS2 on CLx exit</a>	--	<a href="#">30</a>	<a href="#">μs</a>

## (g). Table 4-72 – Logical Layer Timing Parameters (Version 1.0 & 2.0)

To Text:

Parameter	Description	Min	Max	Units
tWarmUpCL2	When exiting CL2 state, time between receiving the first LFPS cycle and sending the first LFPS.	--	<a href="#">100250</a>	μs

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## In the USB4 retimer spec:

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### 4.6 Timing Parameters:

#### To Text:

Parameters	Description	Min	Max	Units
tOBCL1ForwardLFPS	The recommended LFPS forwarding time of an On-board Re-timer when exiting CL1 or CL0s	-	10	us
tOBCL2ForwardLFPS	The recommended LFPS forwarding time of an On-board Re-timer when exiting CL2	-	20	us

#### 4.2.4.3.2.1 CL0s Exit:

##### To Text:

1. Send LFPS on the corresponding transmitter that is in CL0s as follows:
  - In a Cable Re-timer, the first LFPS cycle shall be transmitted tCL1ForwardLFPS time after the first cycle of LFPS on the receiver. It is recommended that an on board retimer will forward the LFPS within tOBCL1ForwardLFPS time after the first cycle of LFPS.

#### 4.2.4.3.2.2 CL1/CL2 Exit:

##### To Text:

This section describes Re-timer behavior during CLx exit for a Gen 4 Link. tCLxForwardLFPS refers to using tCL1ForwardLFPS if the Re-timer is in CL1 and tCL2ForwardLFPS if the Re-timer is in CL2. tWarmUpCLx refers to using tWarmUpCL1 if the Re-timer is in CL1 and tWarmUpCL2 if the Re-timer is in CL2. CL1 and CL2 exit sequences are triggered by LFPS reception where the Re-Timer performs on each of its ports LFPS handshake followed by Gen 4 TS1 and Gen 4 TS2 handshakes separately before moving to Clock Switching on both ports. Figure 4-8 Illustrates an LFPS handshake for a Cable Re-Timer with Ports A and B, and being presented as a reference for demonstrating the sequence rules below. In this example the Re-Timer channels are in CL1 while Port B detects LFPS.

It is recommended for an On-board Re-timer to forward LFPS within tOBCL1ForwardLFPS or tOBCL2ForwardLFPS time for CL1 or CL2 exit accordingly, after receiving the first cycle of LFPS.